AQ533

Ultra-Low Dropout 500mA Voltage Regulator

Product Specification | Revision 1.7 | September 13, 2006

General Description

The AQ533 is an ultra-low dropout voltage regulator capable of delivering **500 mA** to the load. It is adjustable and can set a precise voltage from 1.22V to 12V with two external resistors. The AQ533 meets all specifications down to 1.22V output, unlike CMOS LDO's which loose performance with outputs below 2.25V.

The **enable** pin provides a remote turn-off for low power consumption. It draws virtually zero current in shutdown mode and implements Sequential, Ratiometric, or Simultaneous sequencing schemes. This also allows for a separate bias connection from the pass transistor in order to achieve **ultra low dropout** from VIN to VOUT.

Reverse current protection blocks current flowing from VOUT to VIN when the AQ533 is disabled. No current flows.

To assure accuracy within **1.5% over temperature**, the heart of the AQ533 is a self-correcting AcuRef™ bandgap reference.

On-chip current limit and thermal shutdown with hysteresis protects against any combination of overload and ambient temperature that might cause the junction temperature to exceed safe limits.

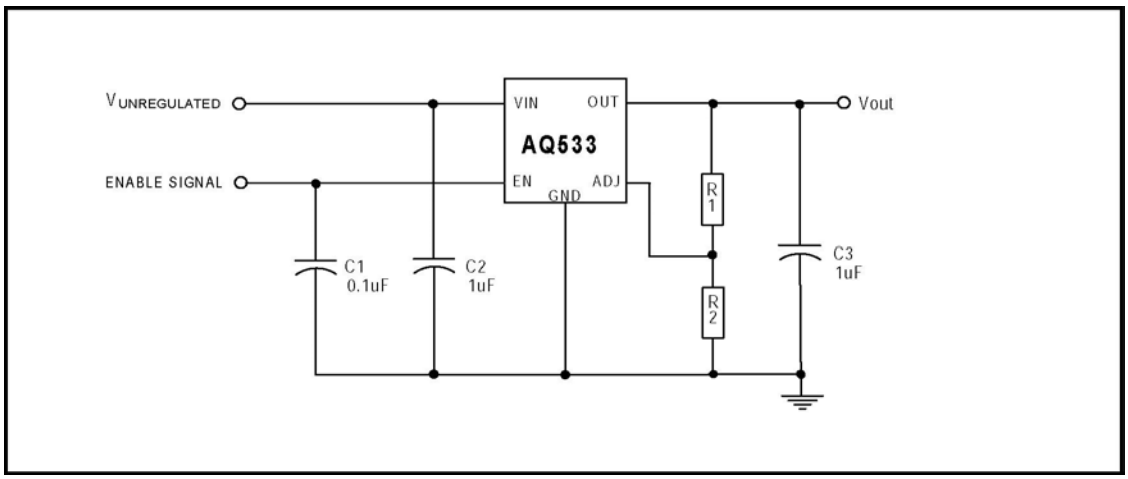
Applications

- Graphic cards
- PC motherboards
- Cell Phones
- DVD video player

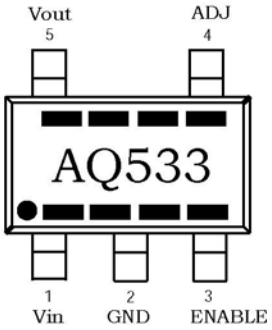
Features

- Low dropout voltage (350mV at **500 mA**)
- Enable pin implements sequencing
- Reverse current protection
- Vout tolerance less than **1.5%** over temperature
- Featured in the very small **SOT-23** package
- Stable with low cost 1µF capacitor
- Low ground current <100 µA
- Thermal protection with hysteresis
- Short circuit protection
- **RoHS compliant** available

Typical Application



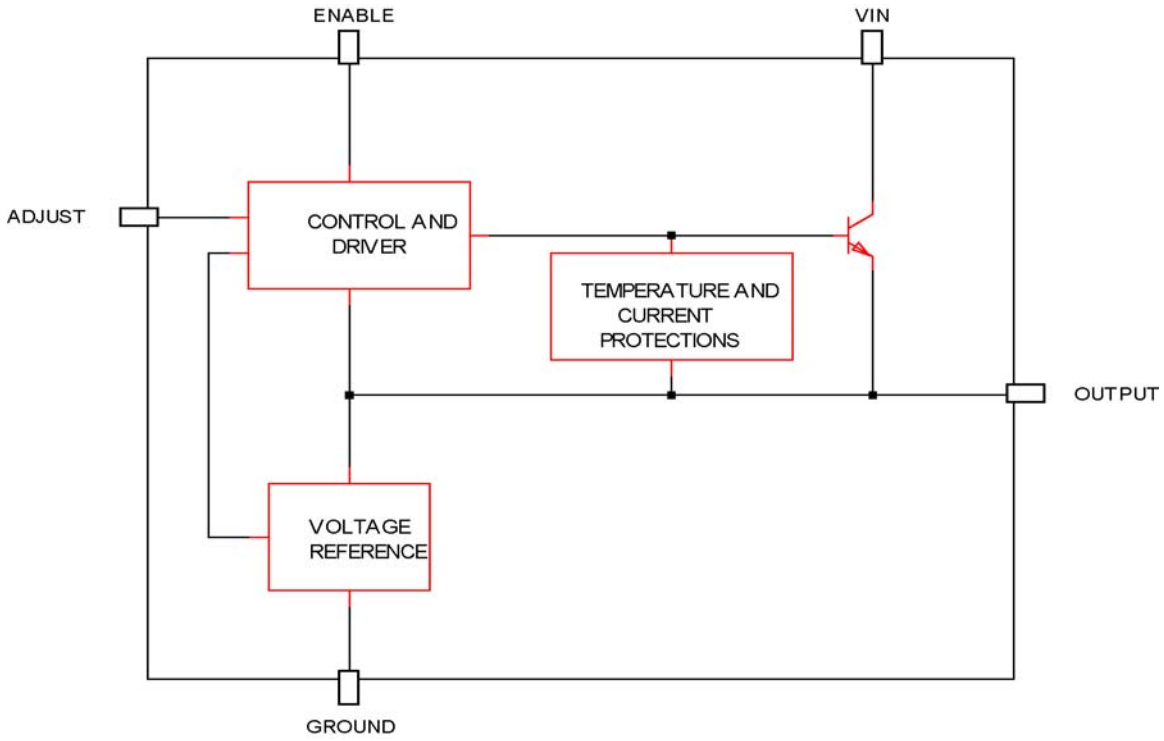
Pin Configuration



Pin Descriptions

Pin Name	Function
VIN	+ Unregulated Input Voltage, Collector of Pass Transistor
Ground	- Ground
ENABLE	Active high, ENABLE > (0.95V + VOUT), Chip bias circuit supply OFF low, ENABLE < 0.25V
Adjust	Adjust input. Connect to resistive feed back divider.
VOUT	Regulated Output

Functional Block Diagram



Ordering Information

Device	Operating Tj	%Tol	PKG Type	VOUT	Wrap	Ordering Number
AQ533	0C° ≤ 125C°	1.0	SOT-23-5	1.8V	T&R	AQ533CY-M5-18-TR
AQ533	0C° ≤ 125C°	1.0	SOT-23-5	1.8V	T&R	AQ533CY-M5-18-TRL
AQ533	0C° ≤ 125C°	1.0	SOT-23-5	2.5V	T&R	AQ533CY-M5-25-TR
AQ533	0C° ≤ 125C°	1.0	SOT-23-5	2.5V	T&R	AQ533CY-M5-25-TRL
AQ533	0C° ≤ 125C°	1.0	SOT-23-5	3.3V	T&R	AQ533CY-M5-33-TR
AQ533	0C° ≤ 125C°	1.0	SOT-23-5	3.3V	T&R	AQ533CY-M5-33-TRL
AQ533	0C° ≤ 125C°	1.0	SOT-23-5	ADJ	T&R	AQ533CY-M5-AJ-TR
AQ533	0C° ≤ 125C°	1.0	SOT-23-5	ADJ	T&R	AQ533CY-M5-AJ-TRL

Note: The TRL parts are Lead Free and RoHS compliant.

Absolute Maximum Ratings

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These stress ratings only, and functional operation of the device at these or any conditions beyond those indicated under recommended Operating Conditions is not implied. Exposure to "Absolute Maximum Rating" for extended periods may affect device reliability. Use of standard ESD handling precautions is required.

Parameter	Value	Units
Maximum VIN	18	Volts
Maximum VENABLE	18	Volts
Power Dissipation (Internally limited)		
Maximum Junction Temperature	150	°C
Operating Junction Temperature Range	0 to 125	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 4 sec.) SOT- 23-5 package	300	°C

Thermal Management

Thermal Resistance (Junction to Ambient)	Typical Value	Units
SOT-23-5 (minimum foot print)	220	°C/W

Thermal Resistance (Junction to Ambient)	Typical Value	Units
SOT-23-5 (Soldered to 1 in^2 1 oz. copper PCB)	170	°C/W

Electrical Specifications

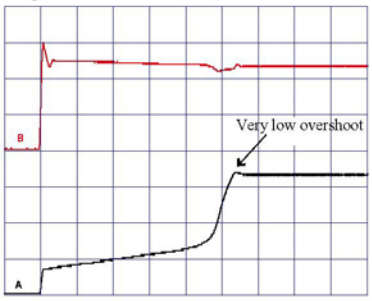
Electrical characteristics are guaranteed over the full temperature range 0ºC <Tj< 125ºC. Ambient temperature must be de-rated based upon power dissipation and package thermal characteristics. Unless otherwise specified: V_{ENABLE} = V_{IN} = (V_{OUT} + 1.5V), I_{OUT} = 10 mA, Tj = 25C. Values in **bold** are over the full temperature range.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VOUT	Output Voltage (1)		-1	V_{OUT}	+1	%
		0°C ≤Tj ≤ 125°C	**-1.5**	V_{OUT}	**+1.5**	%
LNREG	Line Regulation (1)	ΔV_{EN} = V_{OUT} + (1.5V to 10V)		0.035	**0.2**	%
LDREG	Load Regulation (1)	ΔI_{OUT} = (10mA to 500 mA)		0.2	**0.4**	%
VD	Dropout Voltage (1, 2)	I_{OUT} = 100 mA		50	**80**	mV
		I_{OUT} = 250 mA		150	**200**	mV
		I_{OUT} = 500 mA		300	**350**	mV
ISC	Current Limit (1)	V_{EN}-V_{OUT} = 2V	600	800		mA
I_{GND}	Ground Current ON			100	**150**	µA
I_{GND}	Ground Current ON (5)	Adjustable version		65	**80**	µA
VIL	Enable Pin Voltage (OFF)	With respect to GND	**0.25**	0.45		V
VIH	Enable Pin Voltage (ON)	With respect to V_{OUT}		0.92	**0.95**	V
I_{EN}ON	Enable Current ON	I_{OUT} = 10 mA		0.3	**0.5**	mA
		I_{OUT} = 250 mA		1.8	**3.0**	mA
		I_{OUT} = 500 mA		3.8	**5.0**	mA
V_{ADJ}	Reference Voltage	Adjustable version only	1.208	1.220	1.232	V
		0°C ≤Tj ≤ 125°C	**1.202**		**1.238**	V
I_{QMIN}	Minimum Load Current (5)	To maintain regulation		0.5	**2.0**	mA
TC	Temperature Coefficient			**0.005**		%/°C
TS	Temperature Stability			**0.5**		%/°C
V_N	RMS Output Noise (3)			0.003		% V_{OUT}
PSRR	Ripple Rejection Ratio (4)	Vin = 5V	**60**	72		dB
TSD	Thermal Shutdown	Junction Temperature		**150**		°C
TSD_{HYST}	TSD Hysteresis			**25**		°C

Notes: (1) Low duty cycle pulse testing with Kelvin connections required.
(2) Measure (V_{IN} - V_{OUT}) when ΔV_{OUT}, OR ΔV_{REF} = 1%
(3) Bandwidth of 10Hz to 10kHz
(4) 120Hz input ripple
(5) Adjustable version only

Application Notes

Output Overshoot With Line, 500mA Load

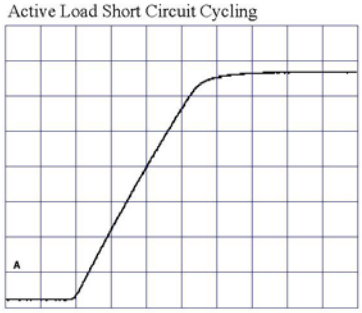


Input Step (B) 0-5V
Output Response (A) 0-3.3V with 500mA load
Horizontal: 100us/div

Output Overshoot With Line, No Load

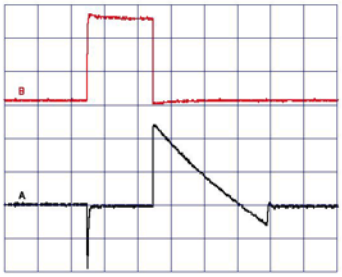
Input Step (B) 0-5V
Output Response (A) 0-3.3V Zero Load
Horizontal: 20us/div

Active Load Short Circuit Cycling



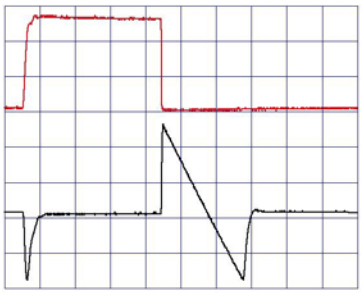
Output Response (A)
Low duty cycle, repetetive, no thermal limit intervention
Horizontal: 10us/div Vertical: 500mV/div

Load Step 0mA to 500mA



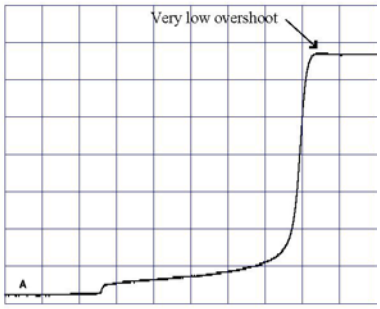
Load Step (B) 0mA to 500mA to 0mA
Output Response (A) 50mV/div (AC coupled)
Horizontal: 500us/div

Load Step 10mA to 500mA



Load Step (B) 10mA to 500mA to 10mA
Output Response (A) 50mV/div (AC coupled)
Horizontal: 100us/div

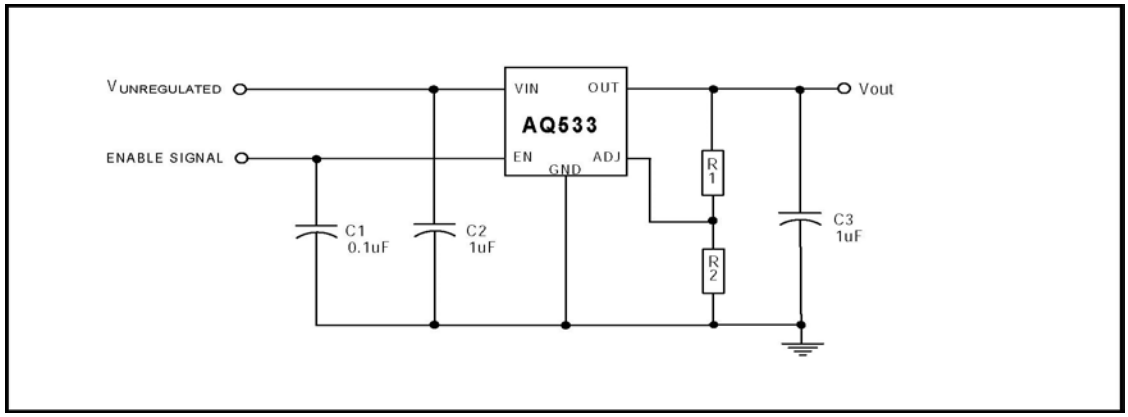
Short Circuit Removal (to no load)



Output Response (A) 0-3.3V
Output grounded to open circuit, single shot
Horizontal: 200us/div Vertical: 500mV/div

Application Notes

1. Typical Application



Notes:

1. Output voltage is 1.22V * (R1 +R2)/R2
2. Input and output capacitors should be located close to the device.
3. The AQ533 will remain stable with C1 and C3 as low as 0.1 µF and 1.0 µF respectively. Overall transient performance is improved with increased capacitance and the addition of C2.
4. The output is fully enabled when Enable is 950 mV above the expected VOUT. EN may be driven by either a digital or analog signal to control either turn-on time or to give full control of risetime.
5. Enable, tied to any separate source >0.95V + VOUT, will insure Ultra-low drop out voltage (350mV@ 500mA) from VIN to VOUT. Or, Enable, tied to Vin will support a low drop out voltage (0.95V).

2. Stability

An **Enable** capacitor is recommended. A 100nF capacitor is a suitable input bypass for almost all applications. A larger capacitor is also suitable depending on the cleanliness of the Enable source.

A **Vin** Capacitor is also recommended. A 1µF capacitor is a bypassing for almost all applications. A larger capacitor is also suitable depending on the cleanliness of the VIN source.

The **Output** capacitor is critical in maintaining regular stability. The AQ533 is stable with an output capacitor greater than 1µF. Any increase of the output capacitor will merely improve the loop stability and the load transient response.

Tantalum Capacitors exhibit the best stability over a wide range of loads and are recommended.

3. Output Voltage

The AQ533 meets all specifications down to 1.22V output. It does not suffer from performance degradation issues such as experienced with CMOS LDO's. Drop out voltage will be less than **350 mV at 500 mA** load with the ENABLE pin held greater than 0.95V + Vout,

The AQ533 develops a 1.22V reference voltage between the adjust pin terminal and ground. This voltage is applied across the resistor R2 to generate a constant current (I2). The current

from the adjust terminal could introduce error to the output, but since it is very small (<0.5μA) compared with the current I2 and very constant with line and load changes, the error can be ignored. The constant current I2 then flows through resistor R1 and sets the output voltage to the desired level.

The AQ533 regulates the voltage that appears between its output and ground pins or between its adjust and ground pins. In some cases, line resistances can introduce errors to the voltage across the load. To obtain the best load regulation a few precautions are needed. For example, it is important to minimize the line resistances to the load. So, the load itself should be tied directly to the output terminal on the positive side and directly to the ground terminal on the negative side.

The best performance is obtained with the positive side of the resistor R1 tied near the load and with the ground side of the resistor R2 tied near the ground of the regulator. This will provide remote output sensing which will optimize regulation at the load.

4. Enable/Sequencing

The AQ533 provides an enable function. The EN pin has to be at least 950 mV higher than the output voltage for the device to be fully turned on. When the voltage of the EN pin is low the device is in shutdown mode and it will not draw any current from the VIN terminal.

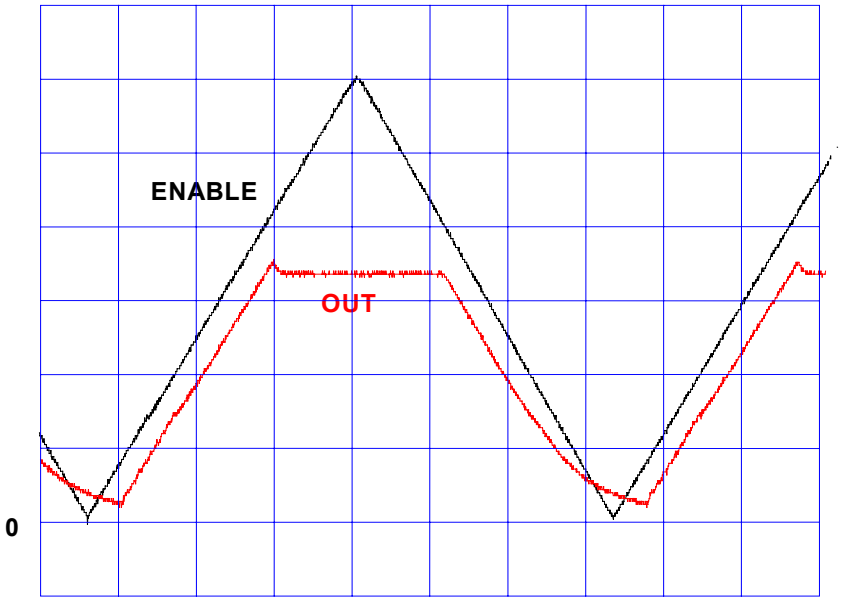


FIG.2 ENABLE 0-5V, Output follows to 3.3V out
(1V/div vertical, 200us/div horizontal)

In addition the enable function includes a sequencing feature, because when the enable pin ramps in voltage the output voltage follows (it will be around 900 mV less than the enable voltage until it reaches the regulation voltage) as shown in Fig. 2 above.

In applications where multiple regulated supply rails are required, it is often required that the relationship between the various supply voltages be controlled during start-up and shutdown. To this end, the AQ533 allows for an analog control of the output voltage via the ENABLE pin. This allows for sequential, ratio-metric and simultaneous sequencing schemes.

5. Reverse Current Protection

The AQ533 provides **Reverse Current Protection**. When the AQ533 is turned off, no current will flow from the output to input. A small current will flow from output to ground through the Vout set resistors R1 and R2. The need for protection diodes is eliminated.

6. Thermal Considerations

When an integrated circuit operates with an appreciable current, its junction temperature is elevated. It is important to quantify its thermal limits in order to achieve acceptable performance and reliability. This limit is determined by summing the individual parts consisting of a series of temperature rises from the semiconductor junction to the operating environment. The heat generated at the device junction flows through the die to the die attach pad, through the lead frame to the surrounding case material, to the printed circuit board, and eventually to the ambient environment.

The AQ533 regulators have internal thermal shutdown to protect the device from over-heating. Under all possible operating conditions, the junction temperature of the AQ533 must be lower than 125°C. A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application.
To determine if a heatsink is needed, the power dissipated by the regulator, P_D, must be calculated:

$$P_D = (V_{IN}-V_{OUT})\, I_L$$

where the I_L is the load current.

The next parameter, which must be calculated, is the max. allowable temperature rise, T(max):

$$T(max)=T_J(max)-T_A(max)$$

where T_J(max) is the maximum allowable junction temperature (125°C), and T_A(max) is the maximum ambient temperature, which will be encountered in the application.
Using the calculated values for T(max) and P_D, the maximum allowable value for the junction to ambient thermal resistance (θ_{JA}) can be calculated:

$$\theta_{JA}=T(max)/\, P_D$$

If the maximum allowable value for θ_{JA} is found to be greater than the junction to ambient thermal resistance for the package used, no heatsink is needed since the package alone will dissipate enough heat to satisfy these requirements.

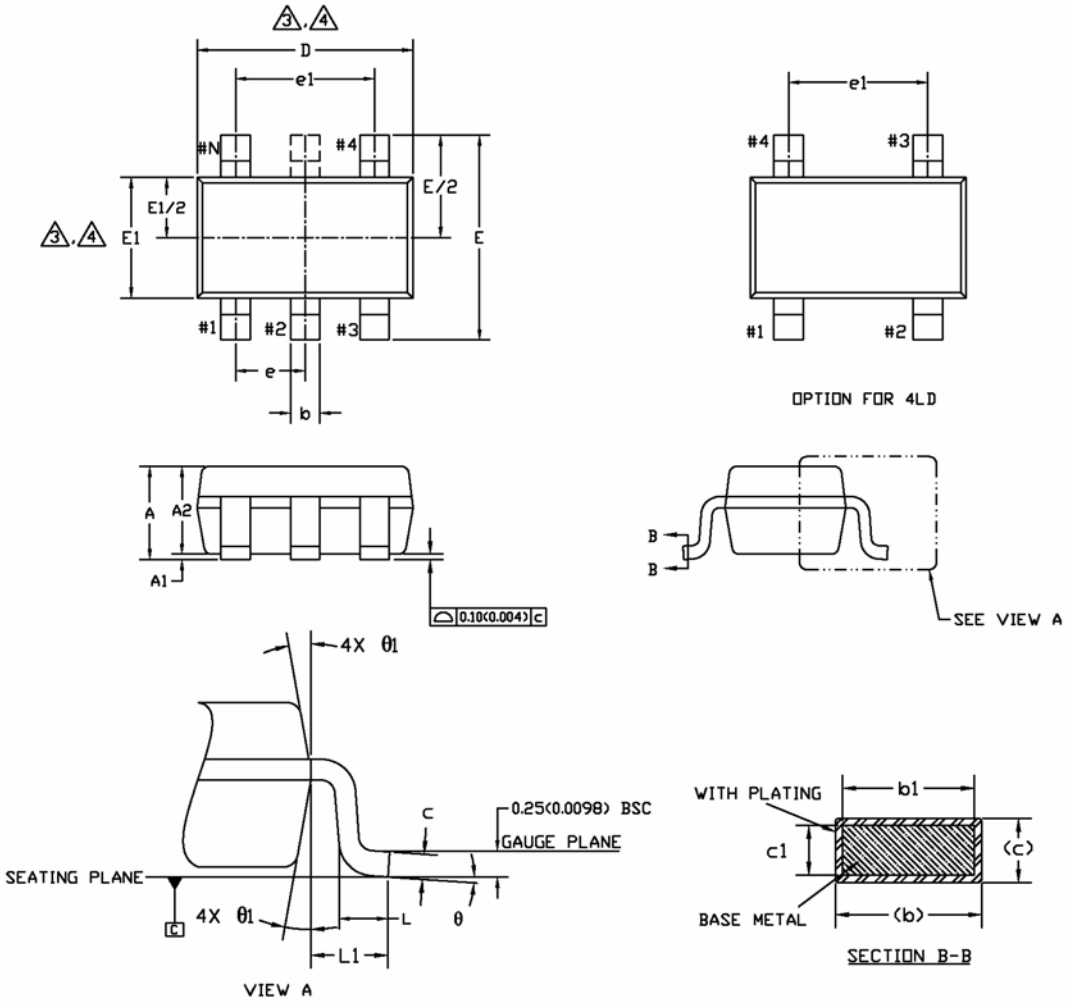
7. Ultra low Dropout Operation

The AQ533 allows for ultra low dropout operation by connecting the pin ENABLE to >0.95V + Vout. This results in a dropout of **350 mV** at **500 mA** of load current, between Vin and VOUT.

This feature is important when the supply voltage is dropping near the output regulated voltage. Furthermore if the voltage dropout is low, the internal power dissipation is also reduced and the thermal requirements of the device are less stringent.

Package Dimensions

PACKAGE DIMENSIONS SOT23-3 SOT23-5, SOT23-4, SOT23-6



SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.20	1.30	1.40	0.047	0.051	0.055
A1	0.05	-	0.15	0.002	-	0.006
A2	0.90	1.15	1.30	0.035	0.045	0.051
b	0.35	-	0.50	0.013	-	0.020
b1	0.35	0.40	0.45	0.013	0.015	0.017
c	0.08	-	0.22	0.003	-	0.008
c1	0.08	0.13	0.20	0.003	0.005	0.007
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.062 BSC		
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.074 BSC		
L	0.35	0.45	0.55	0.013	0.017	0.021
L1	0.60 REF.			0.023 REF.		
θ	0°	4°	8°	0°	4°	8°
θ1	10° TYP			10° TYP		

NOTE :

1. Dimensioning and tolerancing per ASME Y 14.5 M - 1994.
2. Dimensions are in millimeters.Converted inch dimension are not necessarily exact.
3. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.15 mm per side. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 mm per side.
4. Top package may be smaller than the bottom package Dimension D and E1 are determine at the outermost extremes of the plastic body exclusive of mold flash gate burrs and interlead flash.
5. Terminal numbers are shown for reference only. Die is facing up for molding. Die is facing down for trim/form.

Contact Information

Acutechnology Semiconductor Inc.
3487 McKee Rd. Suite 52
San Jose CA , USA 95127

TEL: (408) 259-2300
FAX: (408) 259-9160
website: www.acutechnology.com